

Notice of References Cited	Application/Control No. 09/919,859	Applicant(s)/Patent Under Reexamination MATTAUSCH ET AL.	
	Examiner Pierre M. Vital	Art Unit 2188	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,274,790	12-1993	Suzuki, Hiroaki	711/133
	B	US-			
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	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

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	U	Jude A. Rivers et al., "On High-Bandwidth Data Cache Design for Multi-Issue Processors", IEEE, Dec. 1997
	V	H.J. Mattausch, "Hierarchical Architecture for Area Efficient Integrated N-Port Memories with Latency-Free Multi-Gigabit per Second Access Bandwidth", Electronic Letters, August 1999, Vol. 35, No. 17, Pages 1-2.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.